Low Thermal Impedance MMIC Technology

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***Abstract*— A technology has been developed that reduces the thermal resistance of monolithic microwave integrated circuits (MMIC's). Novel processing techniques are used to fabricate thin-film capacitors and microstrip lines on the back side of the chip. The front side of the chip is metallized to serve as the groundplane; the completed chip is assembled inverted so that the active devices are next to the heat sink, but the chip otherwise is a drop-in replacement for conventional MMIC's. With very conservative deembedding of circuit losses, an AlGaAs/GaAs heterojunction bipolar transistor (HBT) fabricated in this technology achieved record performance at 20 GHz: over 1.2 W output power with 53% power-added efficiency while operating at 12.7 V.**

***Index Terms*— Flip-chip, HBT, MMIC.**

I. Introduction

MONOLITHIC microwave integrated circuits (MMIC's) are being applied to microwave power applications for both military and commercial uses. A key design consideration for MMIC power amplifiers is heat dissipation, since elevated temperatures degrade both the performance and the lifetime of most solid-state devices. GaAs-based MMIC's in particular are constrained in this way because the thermal conductivity of this material is only about one-third that of silicon. Various approaches to improving the thermal characteristics of GaAs MMIC's have been demonstrated, including flip-chip bump assembly [1] and the use of thick-plated airbridges for heat spreading [2]. Flip-chip bump assembly, if applied to MMIC's, requires coplanar circuit techniques that are significantly more complex than standard microstrip circuit designs. The resulting MMIC's also require alignment to custom packages. The airbridge heat-spreading technique is more promising in terms of providing compact power MMIC's. Nevertheless, the area required for the heat-spreading pads is not negligible; furthermore, the common-node inductance associated with the airbridge will degrade the power gain of the device at higher frequencies [3]. A recently published study concluded that the thermal resistance of thermal shunt heterojunction bipolar transistors (HBT's) is inferior to that of flip-chip HBT's [4].

Previously, we reported thermal resistance and microwave power results for discrete, single-finger HBT's fabricated using a low thermal impedance (LTI) process [5]. In this process, the groundplane is placed on the front side of the chip. The chip is assembled inverted so that the emitters are next to the heat sink, while the base and collector are contacted using through-wafer vias. This technique provides low emitter inductance and low thermal resistance without the need for heat-spreading pads. Although good performance was obtained, full MMIC's could not be implemented because no capacitors were available on the same side of the chip as the microstrip transmission lines. Thus, standard L/C matching networks were not practical.

A full MMIC technology has recently been developed based on the LTI process. Novel backside thin-film capacitors have been developed that have dc and radio-frequency (RF) characteristics very similar to conventional frontside capacitors. While the process is immediately applicable to MESFET's, HFET's, and PHEMT's, the MMIC's fabricated to date have used HBT's as the active device. This letter reports record results at 20 GHz using HBT's fabricated in the LTI MMIC technology.

II. LTI MMIC Technology

In the LTI MMIC process, the device active areas and contacts are defined in the same fashion as in a conventional process. TaN patterns are defined to form thin-film resistors, and Ti/Pt/Au metallization is patterned to connect the transistors and resistors as needed and also to form frontside transmission lines. Au is plated to a depth of 3 μm to build up the transmission lines and to form airbridges to the emitters. This plated metal also covers most of the wafer surface to provide a microwave groundplane, except in the immediate vicinity of the resistors, transmission lines, and transistor input and output pads. These nongrounded components are then covered by a 10-μm-thick polyimide layer. A second, unmasked plating step is performed to increase the plated Au thickness to 10 μm. The final processing step on the front side of the wafer is sputter deposition of Au to cover the polyimide; this serves as a low-loss groundplane for the transmission lines that are embedded in the polyimide. The wafer is then mechanically thinned and polished to achieve a thickness of 100 μm while providing a specular backside surface suitable for photolithography.

Four lithographic steps are performed on the backside of the wafer. In the first step, Ti/Pt/Au metallization is deposited on the backside and patterned by liftoff to serve as the bottom plate of thin-film capacitors. Using a low-temperature deposition process to minimize thermal stresses on the thinned wafer, 1500 Å of silicon nitride is deposited to provide the capacitor dielectric. Openings are etched in this nitride layer in the second backside step. The third step is etching of through-wafer vias; the fourth and final lithographic level is a patterned Au plating step. This plated metal provides low-loss microstrip lines and reproducible connections with the nonplanar through-wafer vias, and also serves as the top plate for the backside thin-film capacitors.

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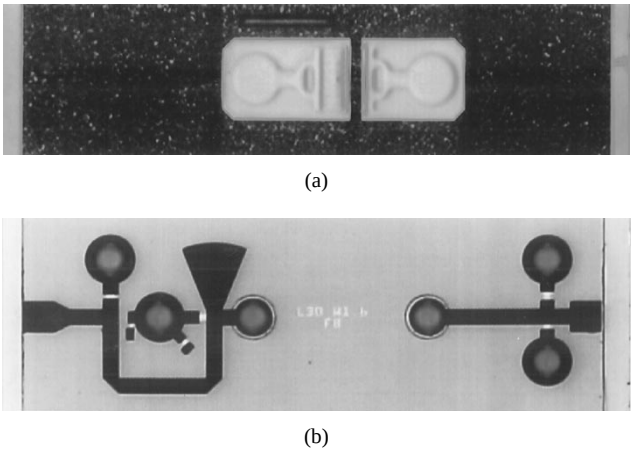

(a)

(b)

Fig. 1. Completed LTI MMIC. (a) Active side. (b) Passive side.

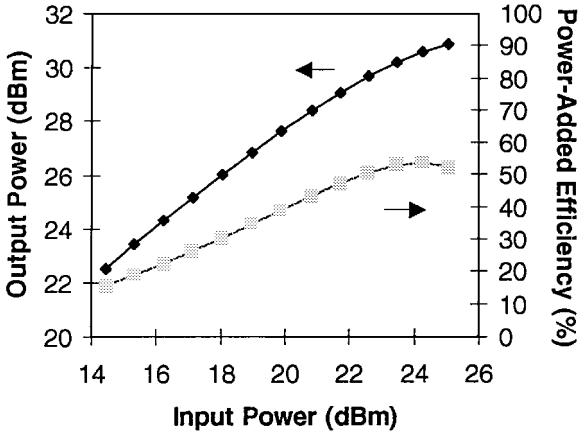

Fig. 2. Output power and PAE of de-embedded HBT at 20 GHz.

The LTI MMIC process therefore has circuit components on both sides of the chip: transistors, resistors, and transmission lines embedded in polyimide on the front side and microstrip lines and thin-film capacitors on the back side. For clarity, the side of the chip that contains the transistors, resistors, and ground plane will be referred to as the "active side," while the other side will be referred to as the "passive side." After processing is completed, the chip is mounted with the active side down against the heat sink, and connections for dc power and RF input/output are made on the passive side of the chip. Note that this configuration makes the flip-chip nature of the MMIC totally transparent to the end user: LTI MMIC's can be designed as drop-in replacements of existing MMIC's, but with significantly lower thermal resistance.

III. Application to High-Efficiency 20-GHz HBT

HBT power amplifiers were chosen to demonstrate the LTI MMIC concept. The HBT material was grown by metal–organic chemical vapor deposition; very heavy base doping of 1×10^{20} cm^{-3} was used to insure adequate power gain at 20 GHz. The LTI MMIC process was used to fabricate multifinger HBT's with matching circuits so that the input and output impedances would be reasonably close to 50 Ω to facilitate accurate load-pull measurements. These circuits were designed for maximum flexibility with respect to device impedance rather than overall minimum loss, and they were implemented on the passive side of the chip. A multipole low-pass topology was designed for the lower-impedance input network, while a two-element network was used for output matching. Fig. 1 shows the active and passive sides of a completed LTI MMIC consisting of an HBT plus pre-matching networks.

A MMIC consisting of an eight-finger HBT unit cell plus matching networks was mounted in a microwave fixture for power testing. Each emitter contact had dimensions of 1.6×30 μm^2. Due to intentional undercutting of the emitter contact to form a self-aligned surface passivation ledge of AlGaAs, the measured active emitter stripe width was actually only 0.8 μm. The center-to-center emitter spacing was 25 μm. Biased at $V_{CE} = 12.7$ V and with a collector current of 132 mA, this circuit achieved an output power of 1.11 W with 4.0 dB gain at 20 GHz, with no circuit losses deembedded. The matching networks were duplicated on the die as separate circuits to allow independent measurement of network losses. At 20 GHz, the minimum losses of the input and output networks were measured as 1.4 and 0.4 dB, respectively (i.e., maximum available gain MAG of -1.4 and -0.4 dB). Note that achieving this minimum loss requires optimum impedances on each side of the matching network, whereas in reality the matching network is in series with the essentially fixed impedance of the device. Actual circuit losses are therefore higher; however, using the minimum loss values gives a very conservative estimate of intrinsic device performance. If these minimum loss values are deembedded, the device performance is conservatively projected to be 1.21 W output power with 53% power-added efficiency (PAE) and 5.8-dB associated gain at 20 GHz. This corresponds to a power density of 5 W/mm of emitter length, and over 6 mW/μm^2 of active emitter area. Fig. 2 shows output power and PAE as a function of input power for this device. To our knowledge, the operating voltage, power density, and the combination of power/efficiency are all state of the art for any solid-state device in this frequency range. Higher operating voltage is preferred because the resulting higher impedance allows matching networks with lower loss, higher combining efficiency, and greater bandwidth. While the LTI devices operated as high as 12.7 V, they were quite rugged at 12 V, with little likelihood of failure during testing even under mismatch conditions. In contrast, conventional HBT devices fabricated with identical epitaxial material from the same epi growth run were unable to operate beyond 10.5 V. Also, the peak power density achieved with a conventional HBT was somewhat lower at 4 W/mm. The reduced thermal resistance of the LTI process therefore appears to improve both device ruggedness and power density.

IV. Conclusion

A novel MMIC process has been demonstrated that places the active device next to the heat sink, yet maintains capability for providing drop-in replacement parts for existing MMIC's. An HBT unit cell fabricated with this process achieved 1.21-W output power with 53% PAE at 20 GHz under 12.7-V operation, based on a very conservative deembedding of circuit

losses. The operating voltage, power density, and ruggedness of the LTI device were all improved compared to conventional HBT's fabricated with the same epitaxial material.

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REFERENCES

[1] H. Sato, M. Miyauchi, K. Sakuno, M. Akagi, M. Hasegawa, J. K. Twynam, K. Yamamura, and T. Tomita, "Bump heat sink technology–-A novel assembly technology suitable for power HBT's," in *1993 GaAs IC Symp. Dig.*, pp. 337–340.

[2] B. Bayraktaroglu, J. Barrette, L. Kehias, C. I. Huang, R. Fitch, R. Neidhard, and R. Scherer, "Very high-power-density CW operation of GaAs/AlGaAs microwave heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 14, pp. 493–495, Oct. 1993.

[3] Y. Amamiya, C.-W. Kim, N. Goto, S. Tanaka, N. Furuhata, H. Shimawaki, and K. Honjo, "Microwave/millimeter-wave power HBT's with regrown extrinsic base layers," in *1994 IEEE Int. Electron Devices Meet. Dig.*, 1994, pp. 199–202.

[4] B. Bayraktaroglu, F. Ali, J. Mason, and P. Smith, "Flip-chip X-band operation of thermally-shunted microwave HBT's with submicron emitters," in *1996 IEEE MTT-S Dig.*, pp. 685–688.

[5] D. Hill, A. Khatibzadeh, W. Liu, T. Kim, and P. Ikalainen, "Novel HBT with reduced thermal impedance," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 373–375, Nov. 1995.